3.3V/5V 3.2Gbps CML LOW POWER LIMITING POST AMPLIFIER w/TTL SD

FEATURES

- Single 3.3V or 5V power supply
- Up to 3.2Gbps operation
- Low noise 50Ω CML data outputs; 60ps edge rates
- 1ps(p-p) max DJ, 1ps(rms) max RJ
- OC-TTL SD output with internal 5kΩ pull-up resistor
- TTL EN input
- Internal input 50Ω termination at inputs and outputs
- Programmable SD level set
- Available in a tiny 10-pin (3mm) MSOP and 16-pin MLF™ (3mm x 3mm) packages

APPLICATIONS

- 1.25Gbps and 2.5Gbps Gigabit Ethernet
- 1062Mbps and 2Gbps Fibre Channel
- 155Mbps, 622Mbps and 2.5Gbps SONET/SDH
- Gigabit interface converter (GBIC)
- Small form factor transceivers
- Parallel 10G Ethernet
- High-gain line driver and line receiver

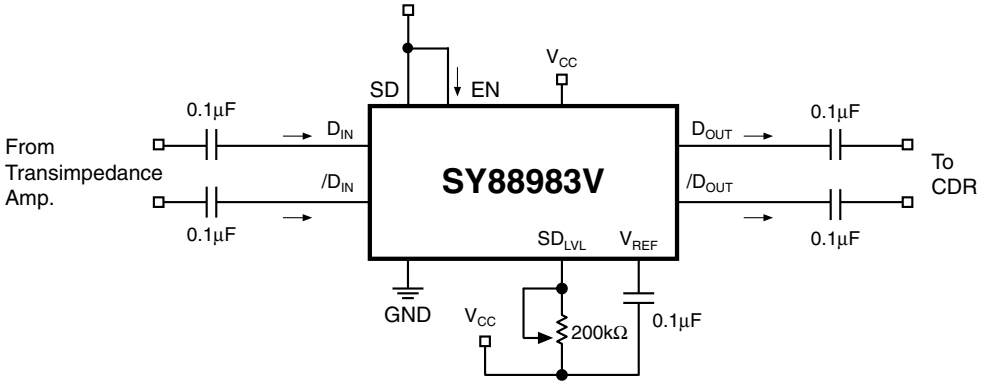
DESCRIPTION

The SY88983V low-power limiting post amplifier is designed for use in fiber optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88983V quantizes these signals and outputs typically 800mVp-p voltage-limited waveforms.

The SY88983V operates from a single +3.3V or +5V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2Gbps and as small as 5mVp-p can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88983V generates a signal detect (SD) open-collector TTL output with internal 5kΩ pull-up resistor. A programmable signal detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss of signal condition. EN deasserts the true output signal without removing the input signal. Typically 4.6dB SD hysteresis is provided to prevent chattering.

TYPICAL APPLICATIONS CIRCUIT



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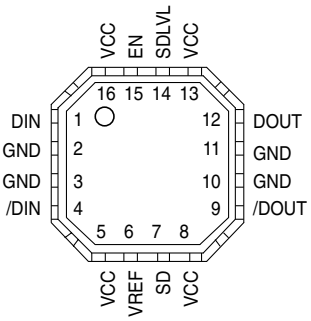
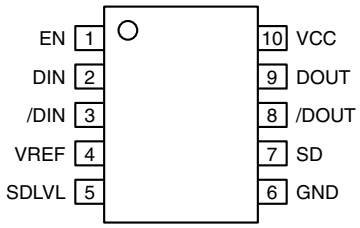
Rev.: A Amendment: /0
Issue Date: December 2002

PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)



10-Pin MSOP (K10-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY88983VKI	K10-1	Industrial	983V
SY88983VKITR*	K10-1	Industrial	983V
SY88983VMI	MLF-16	Industrial	983V
SY88983VMITR*	MLF-16	Industrial	983V

*Tape and Reel

PIN DESCRIPTION

Pin Number (MSOP)	Pin Number (MLF™)	Pin Name	Type	Pin Function
1	15	EN	TTL Input: Default is high.	Enable: Deasserts true data output when low.
2	1	DIN	Data Input	True data input w/50Ω termination to V_{REF}.
3	4	/DIN	Data Input	Complementary data input w/50Ω termination to V_{REF}.
4	6	VREF		Reference Voltage: Placing a capacitor from V_{REF} to V_{CC} helps stablize SD_{LVL}.
5	14	SDLVL	Input: Default is maximum sensitivity.	Signal Detect Level Set: A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which the SD output will be asserted.
6	2, 3, 10, 11, EP	GND	Ground	Device ground.
7	7	SD	Open Collector TTL Output with internal 5kΩ pullup resistor	Signal Detect: Asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
8	9	/DOUT	CML Output	Complementary data output.
9	12	DOUT	CML Output	True data output.
10	5, 8, 13, 16	VCC	Power Supply	Positive power supply.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... 0V to +7.0V
Enable Voltage (EN) ..... 0 to V_{CC}
Signal Detect Level Set Voltage
(SD_{LVL}) ..... (V_{CC} –1.3V) to V_{CC}
Data Input Continuous Current (D_{IN}, /D_{IN}) 1mA
Data Output Current (D_{OUT}, /D_{OUT}) 13mA
Signal Detect Current (SD) 5mA
V_{REF} Current (V_{REF}) 1mA
Storage Temperature (T_S) ..... –55°C to +125°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V or
..... +4.5V to +5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Package Thermal Resistance
MLF™
(θ_{JA}) Still-Air ..... 59°C/W
(ψ_{JB}) Still-Air ..... 32°C/W
MSOP
(θ_{JA}) Still-Air ..... 113°C/W
(ψ_{JB}) Still-Air ..... 74°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current, **Note 1**	3.3V range 5V range		19 21	28 31	mA mA
I_{CC}	Power Supply Current, **Note 2**	3.3V range 5V range		32 38	47 48	mA mA
V_{REF}	V_{REF} Voltage			V_{CC} –1.3		V
SD_{LVL}	SD_{LVL} Level		V_{CC} –1.3		V_{CC}	V
V_{OH}	SD Output HIGH Level	Sourcing 100µA	2.4		V_{CC}	V
V_{OL}	SD Output LOW Level	Sinking 2mA			0.5	V
V_{IH}	EN Input HIGH Voltage		2.0			V
V_{IL}	EN Input LOW Voltage				0.8	V
I_{IH}	EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA
V_{OH}	Output HIGH Voltage	**Note 3**	V_{CC}–0.020	V_{CC}–0.005	V_{CC}	V
V_{OL}	Output LOW Voltage	**Note 3**		V_{CC}–0.400	V_{CC}–0.275	V
V_{OFFSET}	Differential Output Offset				±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω

Note 1. Excludes current of CML output stage. See "*Detailed Description*."

Note 2. Total device current with no output load.

Note 3. Output levels are based on a 50Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V or 4.5V to 5.5V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
HYS	SD Hysteresis	**Note 1**	2	4.6	8	dB
t_{OFF}	SD Release Time			0.1	0.5	µs
t_{ON}	SD Assert Time			0.2	0.5	µs
t_r,t_f	Differential Output Rise/Fall Time (20% to 80%)	**Note 2**		60	120	ps
t_{JITTER}	Deterministic (p-p) Random (rms)	**Note 3**			1 1	ps ps
V_{ID}	Differential Input Voltage Swing		5		1800	mVp-p
V_{IS}	Single-Ended Input Voltage Swing		5		900	mVp-p
V_{OD}	Differential Output Voltage Swing	**Note 4**	550	800		mVp-p
V_{SR}	SD Sensitivity Range		10		50	mVp-p
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
$B_{–3dB}$	3dB Bandwidth			2.2		GHz
S_{21}	Single-Ended Small Signal-Gain		26	32		dB

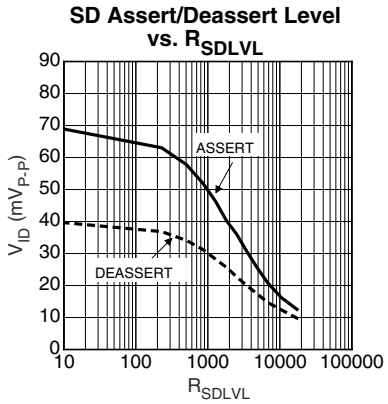
Note 1. Electrical signal.

Note 2. With input signal V_{ID} > 50mVp-p and 50Ω load.

Note 3. Measured using K28.5 pattern at 2.488Gbps, V_{ID} = 100mVp-p

Note 4. Input is a 200MHz square wave, t_r < 300ps, 50Ω load. V_{ID} > 10mVp-p

TYPICAL OPERATING CHARACTERISTICS



DETAILED DESCRIPTION

The SY88983V low power limiting post amplifier operates from a single +3.3V or +5V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as 4mVp-p can be amplified. Figure 1 shows the allowed input voltage swing. The SY88983V generates an SD output, allowing feedback to EN for output stability. SD_{LVL} sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

The SY88983V's inputs are internally terminated with 50Ω to V_{CC} –1.3V. Unless they are not affected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88983V's inputs. Figure 2 shows a simplified schematic of the input stage.

The high sensitivity of the input amplifier allows signals as small as 5mVp-p to be detected and amplified. The input amplifier allows input signals as large as 1800mVp-p. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88983V outputs typically 800mVp-p voltage-limited waveforms for input signals that are greater than 10mVp-p. Applications requiring the SY88983V to operate with high-gain should have the upstream TIA placed as close as possible to the SY88983V's input pins to ensure the best performance of the device.

Output Buffer

The SY88983V's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} or equivalent for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically 800mVp-p waveforms across 25Ω total loads. The output buffer thus switches typically 16mA tail-current. Figure 4 shows the power supply current measurement which excludes the 16mA tail-current.

Signal Detect

The SY88983V generates a chatter-free signal detect (SD) open-collector TTL output with internal 5kΩ pull-up resistor as shown in Figure 5. SD is used to determine that the input amplitude large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss of signal condition. EN deasserts low the true output signal without removing the input signals. Typically 4.6dB SD hysteresis is provided to prevent chattering.

Signal Detect-Level Set

A programmable signal detect-level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} sets the voltage at SD_{LVL}. This voltage ranges from V_{CC} to V_{CC} –1.3V. The external resistor creates a voltage divider between V_{CC} and V_{CC} –1.3V as shown in Figure 6. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from SD_{LVL} to V_{CC}, lowers the SD sensitivity. Hence, larger input amplitude is required to assert SD. *Typical Operating Characteristics* shows the relationship between the input amplitude detection sensitivity and the SD_{LVL} setting resistor.

Hysteresis

The SY88983V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88983V provides typically 2.3dB SD optical hysteresis. As the SY88983V is an electrical device, this datasheet refers to hysteresis in electrical terms. With 4.6dB SD hysteresis, a voltage factor of 1.7 is required to assert or deassert SD.

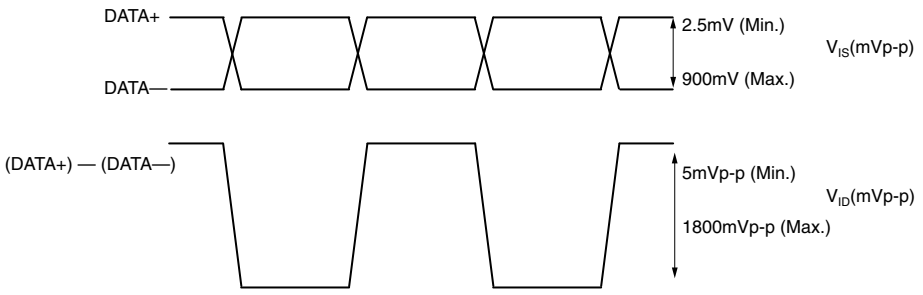


Figure 1. Input Peak-to-Peak (V_{IS}) vs. Input Differential Voltage (V_{ID})

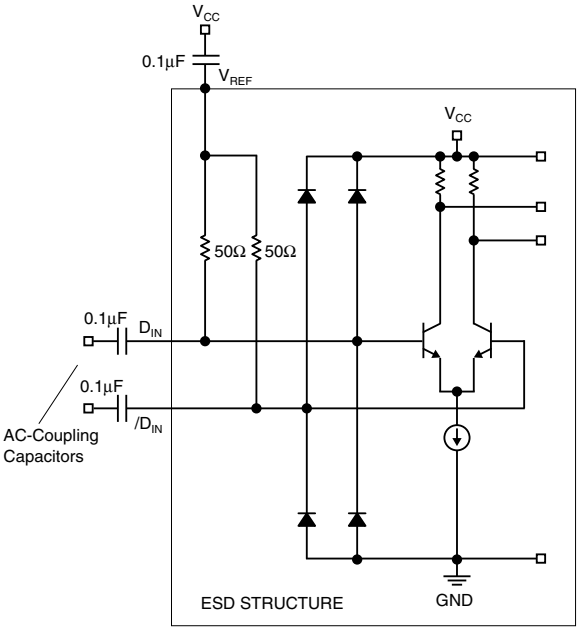


Figure 2. Input Structure

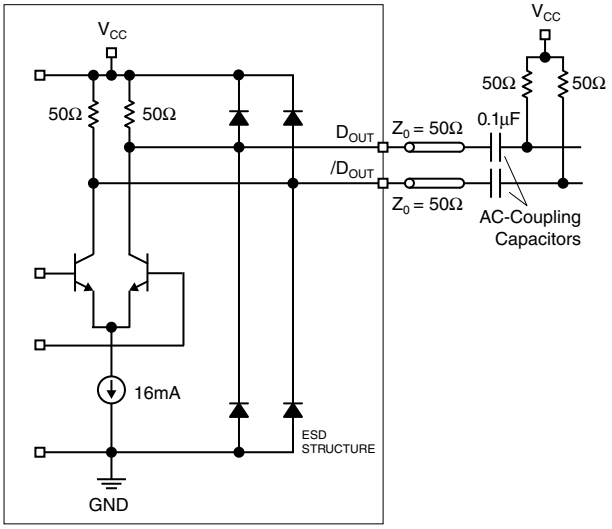


Figure 3. Output Structure

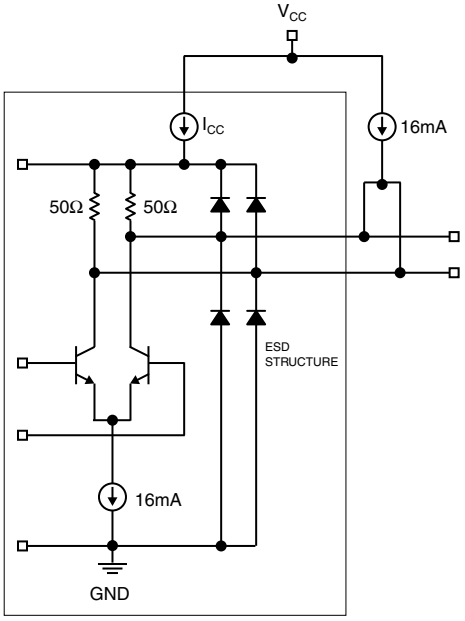


Figure 4. Power Supply Current Measurement

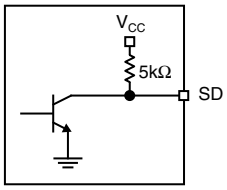


Figure 5. SD Output Structure

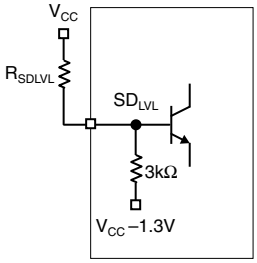
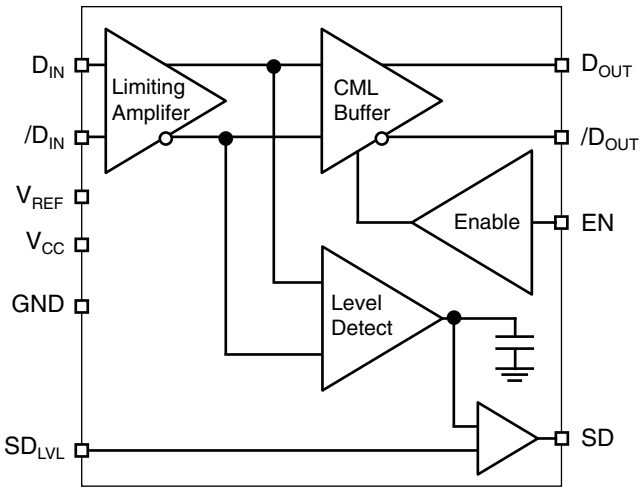


Figure 6. SD_{LVL} Setting Circuit

FUNCTIONAL BLOCK DIAGRAM



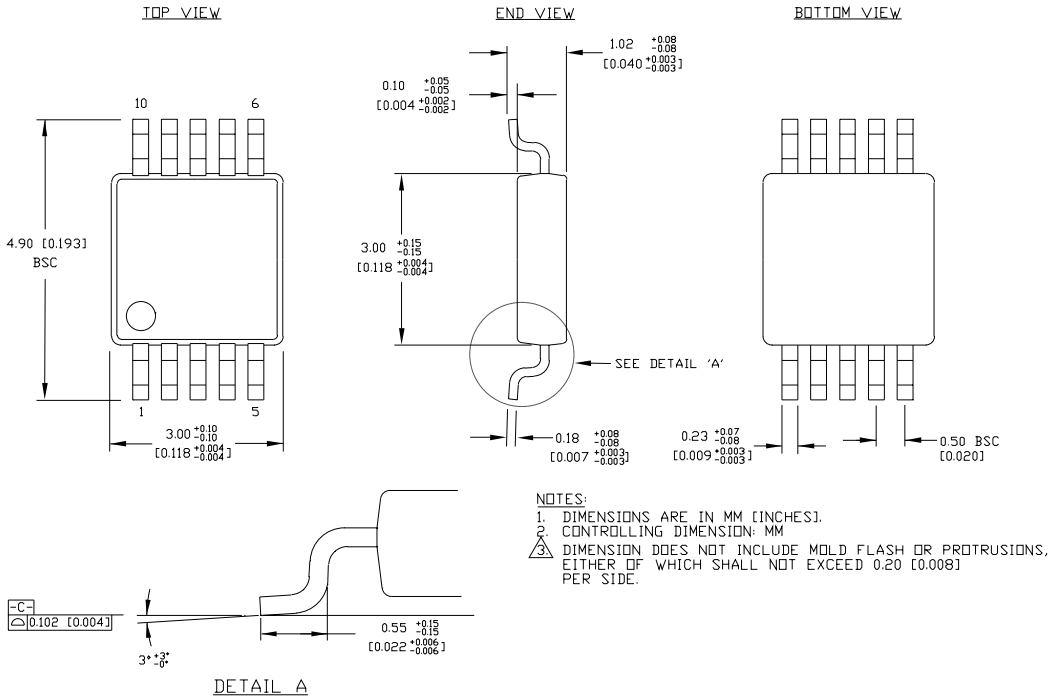
DESIGN PROCEDURE

Layout and PCB Design

Since the SY88983V is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88983V's ground pins should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

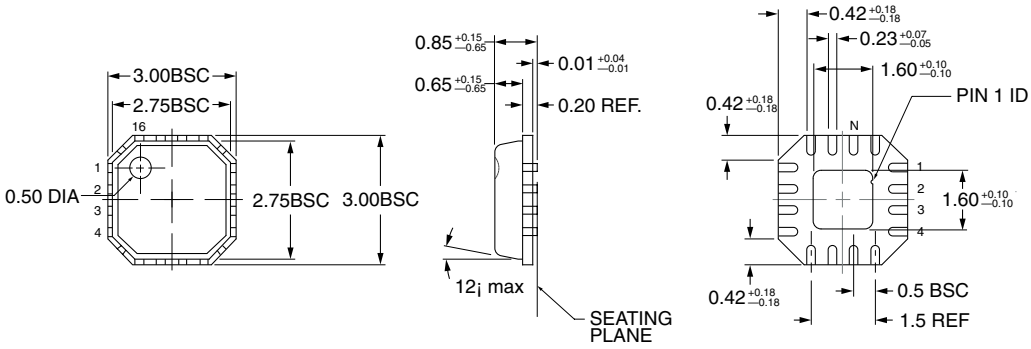
10 LEAD MSOP (K10-1)



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

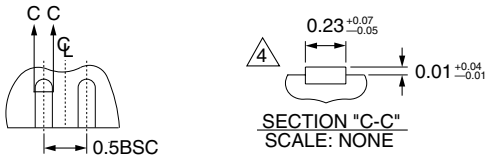
Rev. 00

16 LEAD *Micro*LEAD FRAME™ (MLF-16)



TOP VIEW

BOTTOM VIEW



FOR EVEN TERMINAL/SIDE

1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02

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